CCD44-82 Scientific CCD Sensor Back Illuminated, 2048 x 4096 Pixels, Non-Inverted Mode Operation

INTRODUCTION

These devices offer an image area of 2048 x 4096 pixels. Most devices are offered in a full-frame (FF) architecture, but some variants are supplied with frame transfer (FT) wiring. Back illumination technology, in combination with an extremely low noise amplifier, makes the devices well suited to the most demanding applications, such as astronomy.

The output amplifier is designed to give excellent noise levels at low pixel rates and can match the noise performance of most conventional scientific CCDs at pixel rates as high as 1 MHz. The low output impedance and optional FET buffer simplify the interface with external electronics.

The readout register has a gate-controlled dump-drain to allow fast dumping of unwanted data. The register is designed to accommodate three image pixels of charge and a summing well is provided capable of holding four image pixels. The output amplifier has a feature to enable the responsivity to be reduced, allowing the reading of such large charge packets.

The device is supplied in a package designed to facilitate the construction of large close-butted mosaics and is designed to be used cryogenically. The design of the package will ensure that the device flatness is maintained at the working temperature.

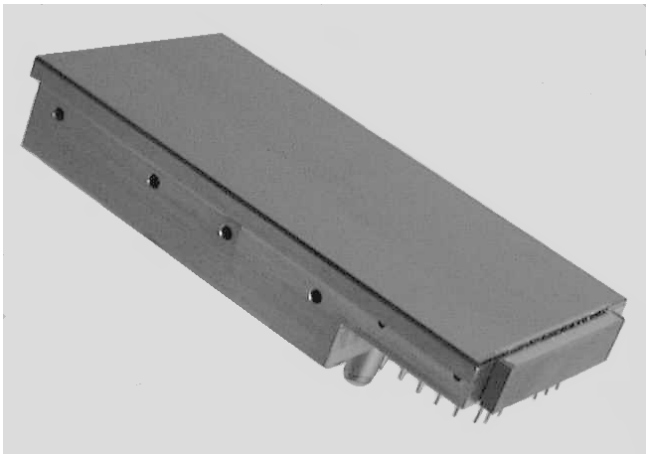
The sensor is shipped in a protective container, but no permanent window is fitted.

PART REFERENCES

CCD44-82-g-xxx

g = cosmetic grade

B23 = NIMO BT Astronomy process Broadband coating
B24 = NIMO BT Astronomy process Broadband coating fringe suppressed
A43= NIMO BT Astronomy process UV coating
C84= NIMO BT Astronomy process no coat
E17= NIMO BT Basic process ER1 coating
D26= NIMO BT DD Astronomy process Midband coating
D03= NIMO BT DD Astronomy process Broadband coating
B43= NIMO BT DD Astronomy process Broadband coating (FT)
D48= NIMO BT DD Astronomy process ER1 coating
D23= NIMO BT DD Astronomy process ER1 coating fringe suppressed
D42= NIMO BT DD Astronomy process 2-layer coating
A72= NIMO BT DD Basic process ER1 coating (FT)



SUMMARY SPECIFICATION

Number of pixels	2048(H) x 4096(V)
Pixel size	15 µm square
Image area	30.7 mm x 61.4 mm
Outputs	2
Package size	31.7 mm x 66.6 mm
Package format	Invar metal package with PGA connector
Focal plane height, above base	14.0 mm
Connectors	PGA
Flatness	20µm p-v
Amplifier responsivity	6.0 µV/e^-
Readout noise	2.5 e^- at 20kHz
Maximum data rate	1 MHz
Image pixel charge storage	200,000 e^-
Dark signal	0.01 e^-/pixel/hour (at 153K)

Quoted performance parameters given above are “typical” values. Specification limits are shown later in this data sheet.

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Template: DF764388A-3
108760

PERFORMANCE (At 173 K unless stated)

Electro-Optical Specification

	Min	Typical	Max	Units	Note
Peak charge storage (image)	150,000	200,000	-	e^-/pixel	1
Peak charge storage (register)	-	600,000	-	e^-/pixel	
Output node capacity: OG2 low (mode 1) OG2 high (mode 2)	 - -	 300,000 1,200,000	 - -	 e^- e^-	 2
Output amplifier responsivity: OG2 low (mode 1) OG2 high (mode 2)	 4.5 -	 6.0 1.5	 - -	 $\mu V/e^-$	
Readout noise	-	2.2	4.0	e^- rms	3
Readout frequency	-	20	1000	kHz	4
Dark signal (at 153 K): standard silicon deep depleted silicon	 - -	 0.01 0.02	 1.00 2.00	 e^-/pixel/h	 5
Charge transfer efficiency: parallel serial	 99.9990 99.9990	 99.9995 99.9998	 - -	 % %	 6

NOTES

1. Signal level at which resolution begins to degrade.
2. Operation of the OG2 gate modified the output node. OG2 low (mode 1) is normally used for low noise high responsivity.
3. Measured with correlated double sampling at 20 kHz pixel rate with OG2 =OG1 + 1 V.
4. Depending on the external load capacitance to be driven. The register will transfer charge at higher frequencies, but performance cannot be guaranteed.
5. Dark signal is typically measured at 173 K with the substrate voltage at +9.0 V for standard silicon (4 V for deep depleted silicon). It is a strong function of temperature and the typical average (background) dark signal is taken as:

   $Q_d/Q_{do} = 122T^3e^{-6400/T}$

   where Q_{do} is the dark current at 293 K.
6. Measured with a ^{55}Fe X-ray source.

COSMETIC SPECIFICATIONS

Maximum allowed defect levels are indicated below.

Standard Silicon

Grade	0	1	2
Column defects: (black or white)	2	6	12
White spots	250	500	1000
Total spots (black and white)	750	1250	2000
Traps > 200e-	20	30	50

Deep Depleted Silicon

Grade	0	1	2
Column defects: (black or white)	2	6	12
White spots	500	1000	1500
Total spots (black and white)	1250	2000	3000
Traps > 200e-	20	30	50

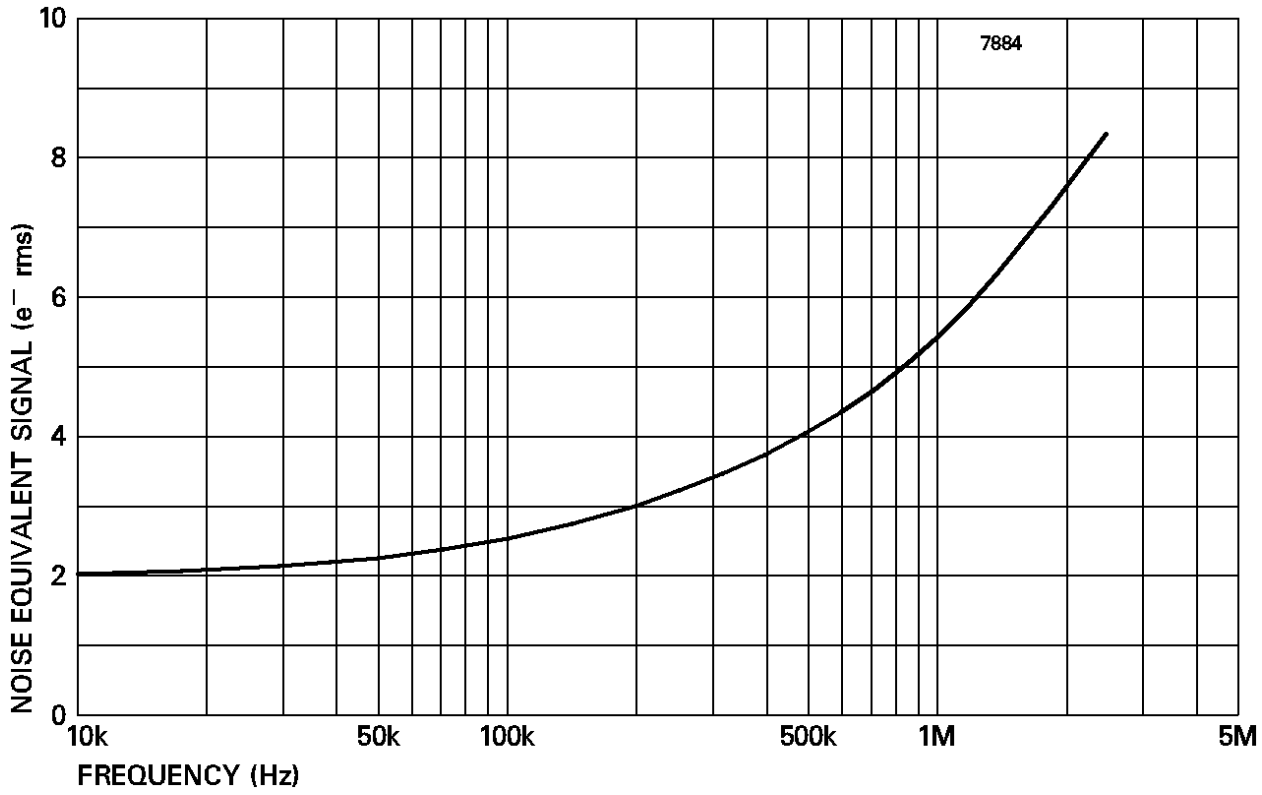
Grade 5 devices are fully functional but with an image quality below that of grade 2, and may not meet all other specifications. Not all parameters may be tested.

DEFINITIONS

White spots	A defect is counted as a white spot if the dark generation rate is more than 100 e^-/pixel/h at 153 K (typically measured at 173 K). The typical temperature dependence is given by $Q_d/Q_{do} = 122 \times T^3 e^{-6400/T}$
Black spots	A black spot defect is a pixel with a response less than 80% of the local mean signal.
Column defects	A column is counted as a defect if it contains at least 100 white or dark single pixel defects.
Traps	A trap causes charge to be temporarily held in a pixel and these are counted as defects if the quantity of trapped charge is greater than 200 e^- at 173 K

TYPICAL OUTPUT AMPLIFIER NOISE

The variation of typical read noise with operating frequency is shown below (measured using correlated double sampling with a pre-sampling bandwidth equal to twice the pixel rate in mode 1 at approximately 173 K).



SPECTRAL RESPONSE AT 173 K

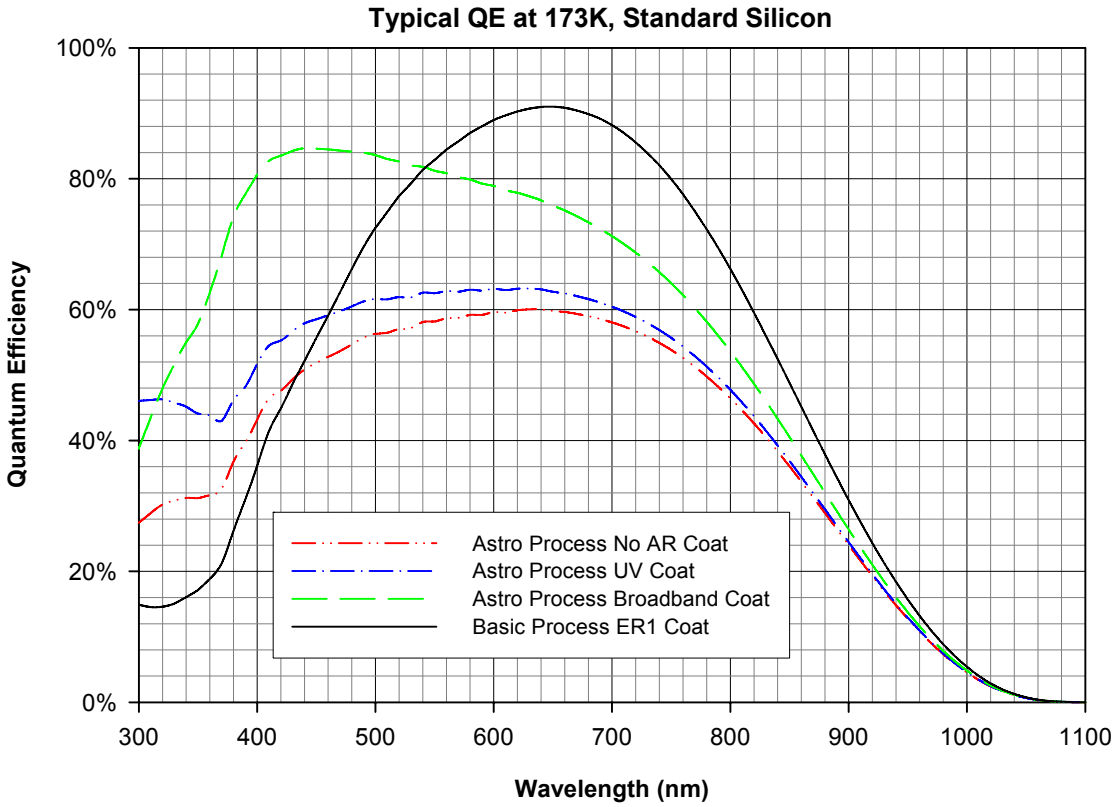
STANDARD SILICON

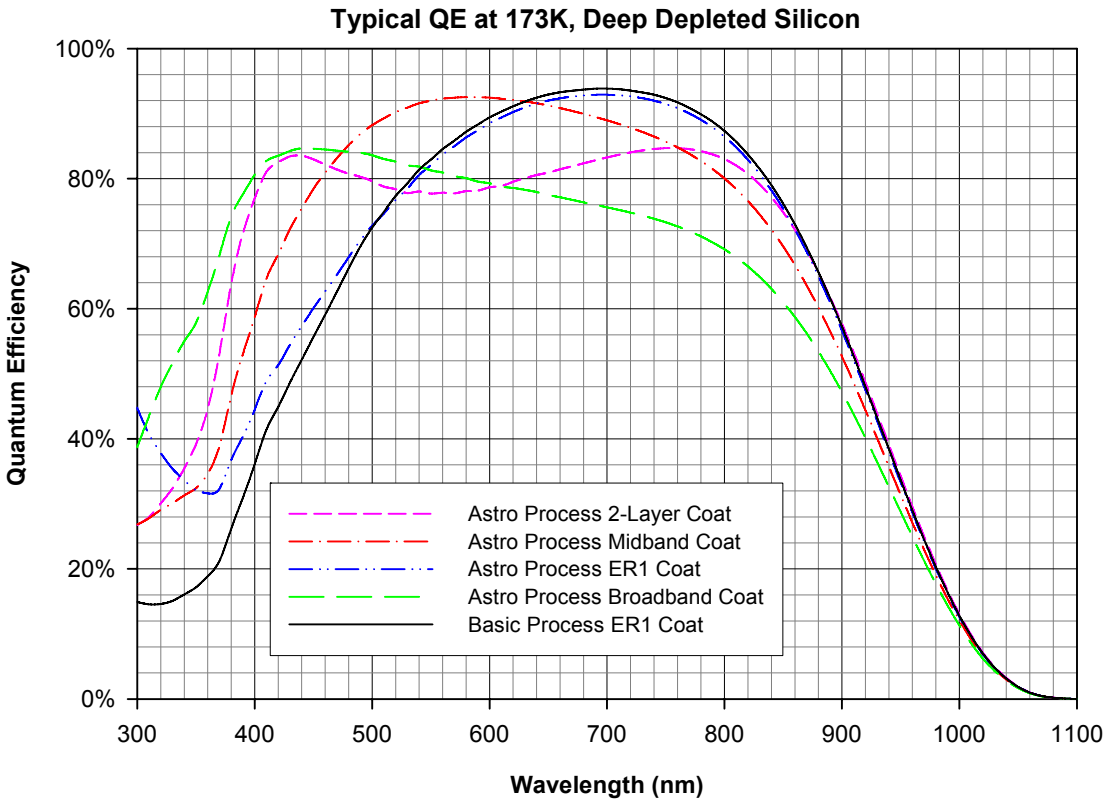
	Astronomy Process Broadband Coated	Astronomy Process UV Coated	Astronomy Process No AR Coating	Basic Process ER1 Coating	Maximum Pixel Response Non-Uniformity PRNU (1σ) (%)
Wavelength (nm)	Minimum QE (%)	Minimum QE (%)	Minimum QE (%)	Minimum QE (%)	Maximum (%)
350	40	37	-	10	-
400	70	48	-	25	3
500	80	60	-	60	-
650	75	60	-	85	3
900	25	20	-	25	5

DEEP DEPLETED SILICON

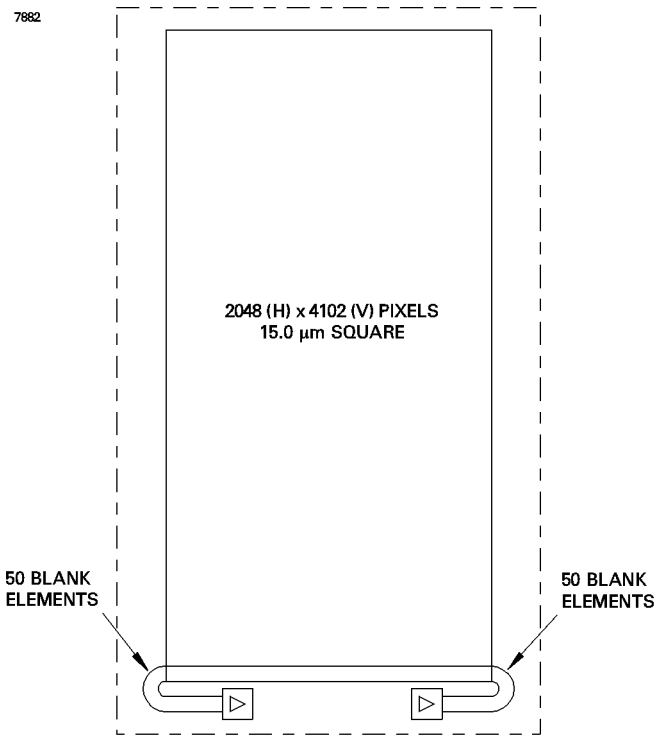
	Astronomy Process Midband Coated	Astronomy Process Broadband Coated	Astronomy Process ER1 Coating	Astronomy Process 2-layer Coating	Basic Process ER1 Coating	Maximum Pixel Response Non-Uniformity PRNU (1 σ) (%)
Wavelength (nm)	Minimum QE (%)	Minimum QE (%)	Minimum QE (%)	Minimum QE (%)	Minimum QE (%)	Maximum (%)
350	20	40	20	30	10	-
400	50	70	35	70	25	3
500	80	75	65	75	60	-
650	80	70	80	75	85	3
900	40	40	45	50	45	5

TYPICAL CURVES

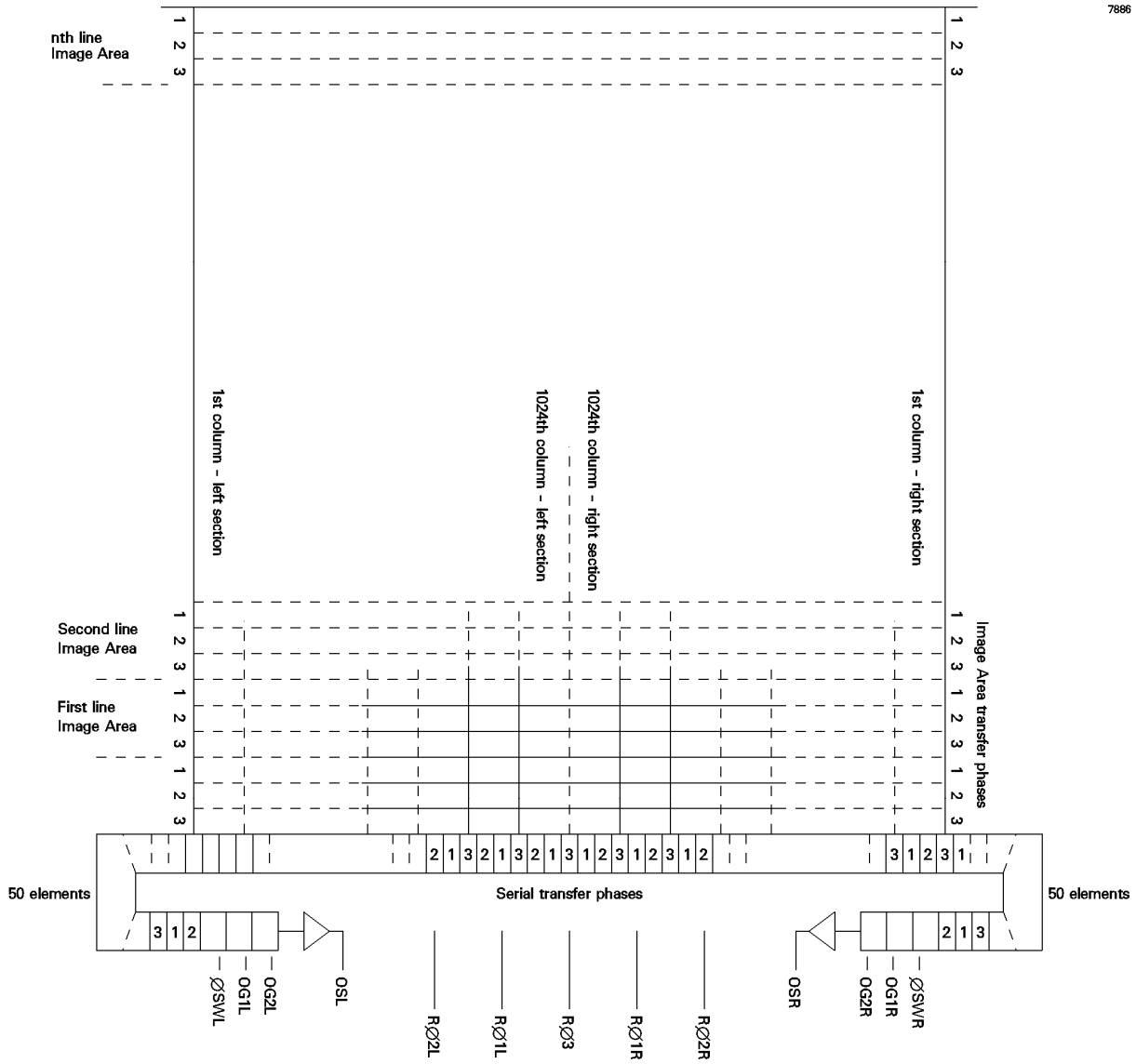




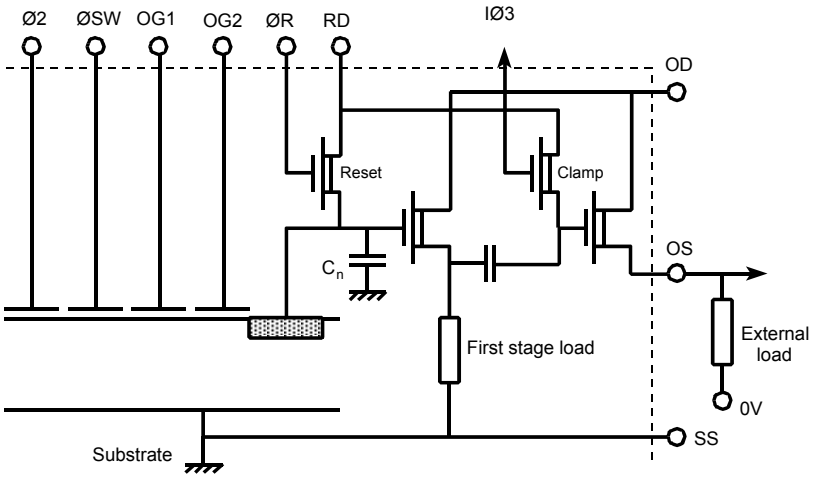
ARCHITECTURE



ARRANGEMENT OF ELECTRODES (full frame only)



OUTPUT CIRCUIT



The output impedance is typically 300 Ω.

The on-chip power dissipation is typically 20 mW.

Optional JFET not shown

ELECTRICAL INTERFACE

CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

The tables below give the pin-outs and clock amplitudes.

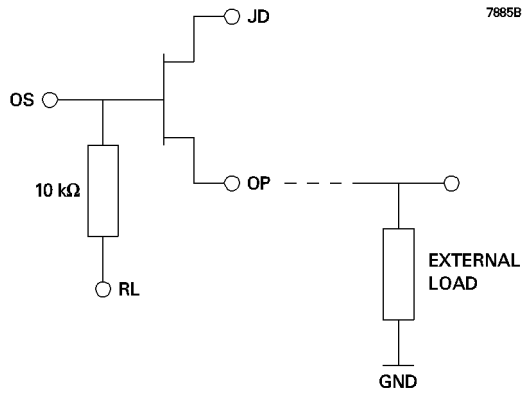
PGA PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 7)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
A1, A8, C1, C8, F2, F7	SS	Substrate	See note 8			-
D8	I∅1	Image clock	8	10	15	±20
E8	I∅2	Image clock	8	10	15	±20
F8	I∅3	Image clock	8	10	15	±20
D4	R∅1 (L)	Register clock	8	11	15	±20
E4	R∅2(L)	Register clock	8	11	15	±20
D5	R∅1 (R)	Register clock	8	11	15	±20
E5	R∅2(R)	Register clock	8	11	15	±20
F6	R∅3	Register clock	8	11	15	±20
E3	∅R (L)	Reset gate	9	12	15	±20
E6	∅R (R)	Reset gate	9	12	15	±20
E2	∅SW (L)	Summing well gate	9	11	15	±20
E7	∅SW (R)	Summing well gate	9	11	15	±20
F3	DG (see note 9)	Dump gate	-0.5	0	15	±20
D3	OG1 (L)	Output gate	1	3	4	±20
D6	OG1 (R)	Output gate	1	2	4	±20
B2	DD (L)	Dump drain	22	24	26	-0.3 to +30
B7	DD (R)	Dump drain	22	24	26	-0.3 to +30
D2	OG2 (L)	Output gate	See note 10			±20
D7	OG2 (R)	Output gate	See note 10			±20
B1	OD (L)	Output drain	27	29	32	-0.3 to +35
B8	OD (R)	Output drain	27	29	32	-0.3 to +35
A2	OS (L)	Output source	See note 11			-0.3 to +25
A7	OS (R)	Output source	See note 11			-0.3 to +25
C2	RD (L)	Reset drain	15	17	19	-0.3 to +25
C7	RD (R)	Reset drain	15	17	19	-0.3 to +25
Optional connection for 309 JFET (see note 12)						
A3	RL (L)	Load resistor	A_{GND}(0 V)			
A6	RL (R)	Load resistor	A_{GND}(0 V)			
B3	OP (L)	JFET source				
B6	OP (R)	JFET source				
C3	JD (L)	JFET drain	OD (L) + 2 V (0 V)			
C6	JD (R)	JFET drain	OD (L) + 2 V (0 V)			
Other connections (Full frame devices only- see note 13)						
D1, F1	Temp	Temperature sensor	PT100			
E1	NC	No Connection				

If all voltages are set to the typical values, operation at, or close to, specification should be obtained. Some adjustment within the minimum-maximum range specified may be required to optimise performance. Refer to the specific device test data if possible.

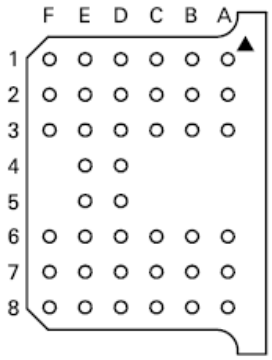
NOTES

7. All pulse low level 0 ± 0.5 V except readout register clocks +1 V
8. Devices can be operated with low substrate (0 V) or higher substrate (9 V). Low substrate is particularly recommended for deep depleted variants, since it optimises depletion depth for best Point Spread Function.
9. Non-charge dumping level is shown. For charge dumping DG should be pulse to 12 ± 2 V
10. OG2 = OG1 + 1 V; for operation in high responsivity, low noise mode, OG2 should be set to +4 V typical. For operation in low responsivity, increased charge handling mode, OG2 should be set to +20 V.
11. 3 - 5 V below OD. Do not connect to voltage supply but use a 3 - 5 mA current source or a 5 - 10 kΩ external load.
12. The JFET is floating, with its gates connected to OS. A floating 10 kΩ load resistor is also connected to OS. The FET may be used to buffer the chip output (OS) if desired; in this case, connect the FET output to A_{GND} via a 5 mA load and RL directly to A_{GND} (U309 data: V_{GD} and V_{GS} absolute maximum = -2 5 V). See detail below.
13. These connections are for full-frame devices only. For frame transfer devices, D1, E1 and F1 are connected to S∅1, S∅2 and S∅3 respectively.

DETAILS OF FET BUFFER



PIN CONNECTIONS (View facing underside of package)



ELECTRICAL INTERFACE CHARACTERISTICS

For Full-Frame Variants Only

Electrode Capacitances (defined at mid-clock level)

	Typical	Units
IØ/IØ inter-phase	20	nF
IØ/SS	50	nF
RØ/RØ	90	pF
RØ/SS	175	pF
ØR/SS	20	pF

Electrode Series Resistance

	Typical	Units
IØ	40	Ω
RØ	10	Ω

The total capacitance on each phase is the sum of the inter-phase capacitance to each of the adjacent phases and the capacitance of the phase to substrate.

POWER UP/POWER DOWN

When powering the device up or down it is critical that any specified maximum rating is not exceeded. Specifically the voltage for the amplifier drains (pins B1 and B8) must never be taken negative with respect to the substrate. Hence, if the substrate is to be operated at a positive voltage (e.g. to minimise dark current) then the drive electronics should have a switch-on sequence which powers up all the drains to their positive voltages before the substrate voltage starts to increase from zero.

It is also important to ensure that excess currents (see note 11) do not flow in the OS or DOS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier.

Similarly, for powering down, the substrate must be taken to zero voltage before the drains.

POWER CONSUMPTION

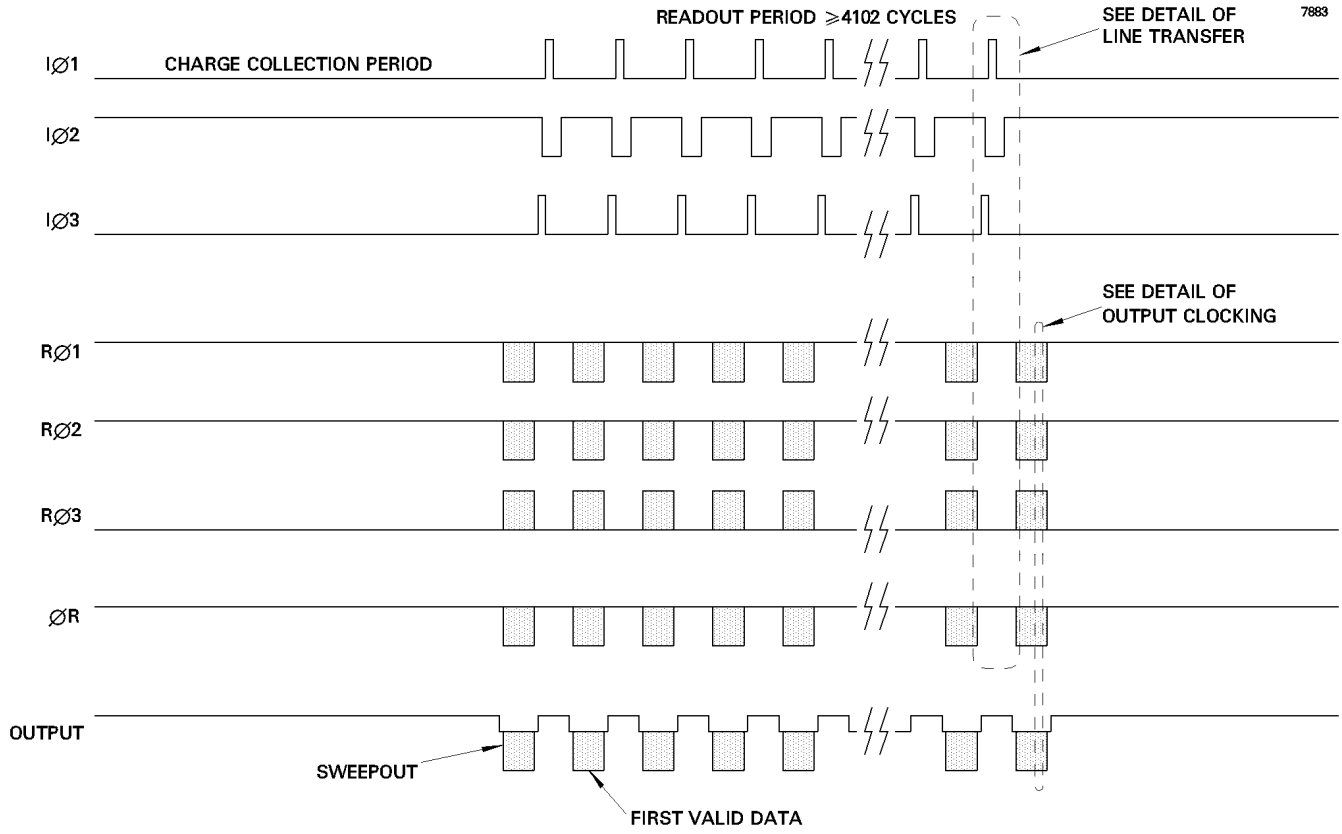
The power dissipated within the CCD is a combination of the static dissipation of the amplifiers and the dynamic dissipation from the parallel and serial clocking (i.e. driving the capacitive loads).

The table below gives representative values for the components of the on-chip power dissipation for the case of a full-frame device with continuous line-by-line read-out using one amplifier. The frequency is that for clocking the serial register and an appropriate value of the amplifier load is utilised in each case.

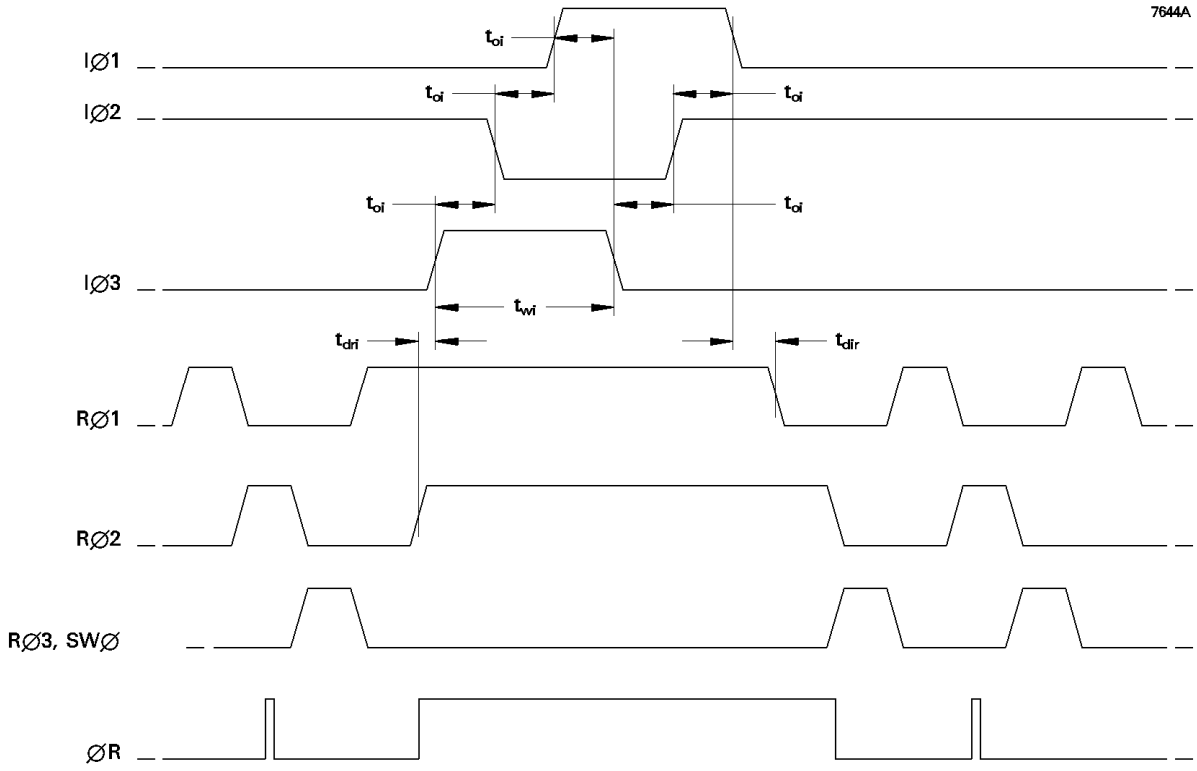
Readout frequency	Line time (ms)	Power dissipation (mW)			
		Amplifiers	Serial clocks	Parallel clocks	Total
100 kHz	40	20	10	1	31
1 MHz	4	20	100	10	130

The dissipation reduces to only that of the amplifiers during the time that charge is being collected in the image sections with both the parallel and serial clocks static.

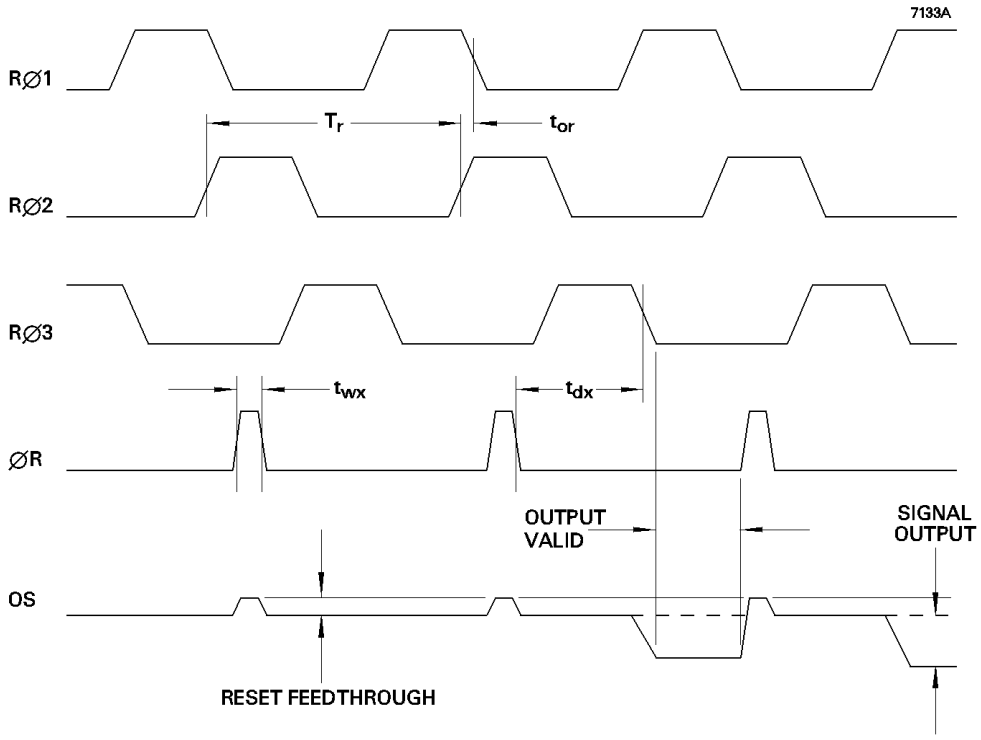
FRAME READOUT TIMING DIAGRAM (Full-Frame Only)



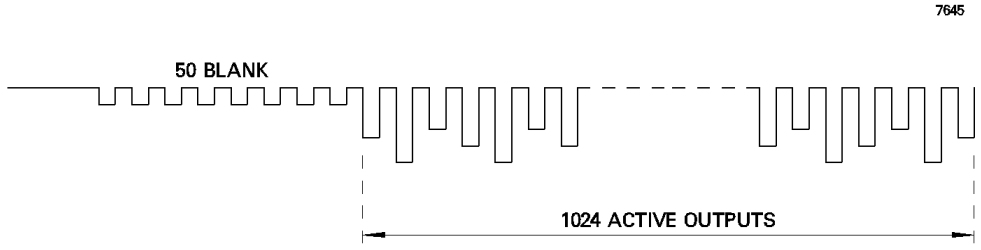
DETAIL OF LINE TRANSFER



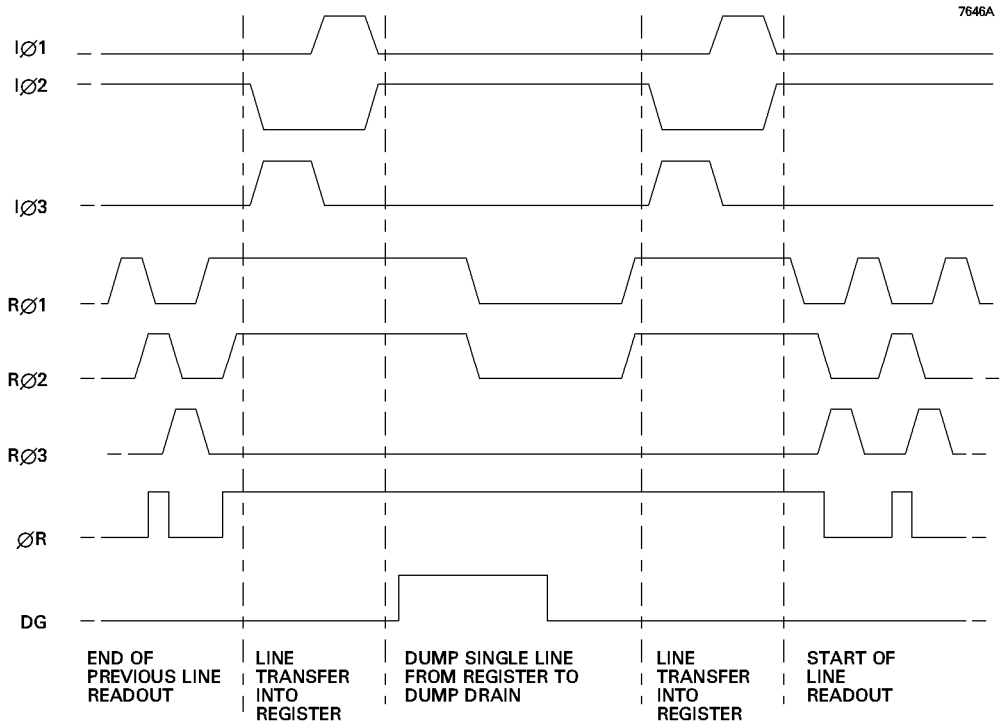
DETAIL OF OUTPUT CLOCKING



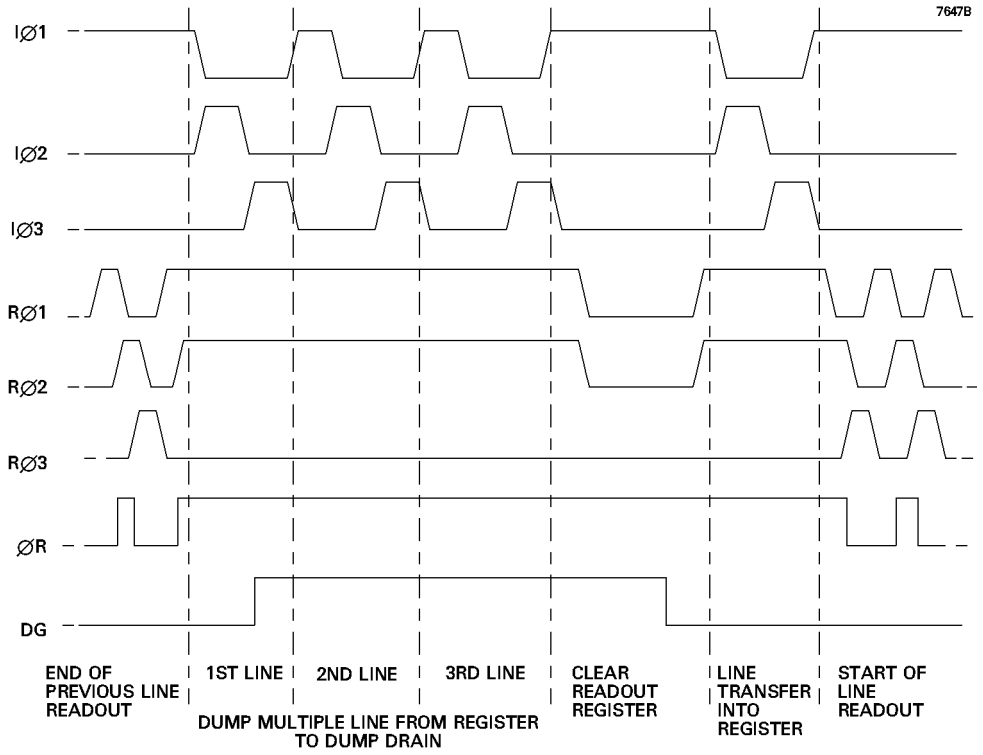
LINE OUTPUT FORMAT



DETAIL OF VERTICAL LINE TRANSFER (SINGLE LINE DUMP) Full-Frame Only



DETAIL OF VERTICAL LINE TRANSFER (MULTIPLE LINE DUMP) Full-Frame Only



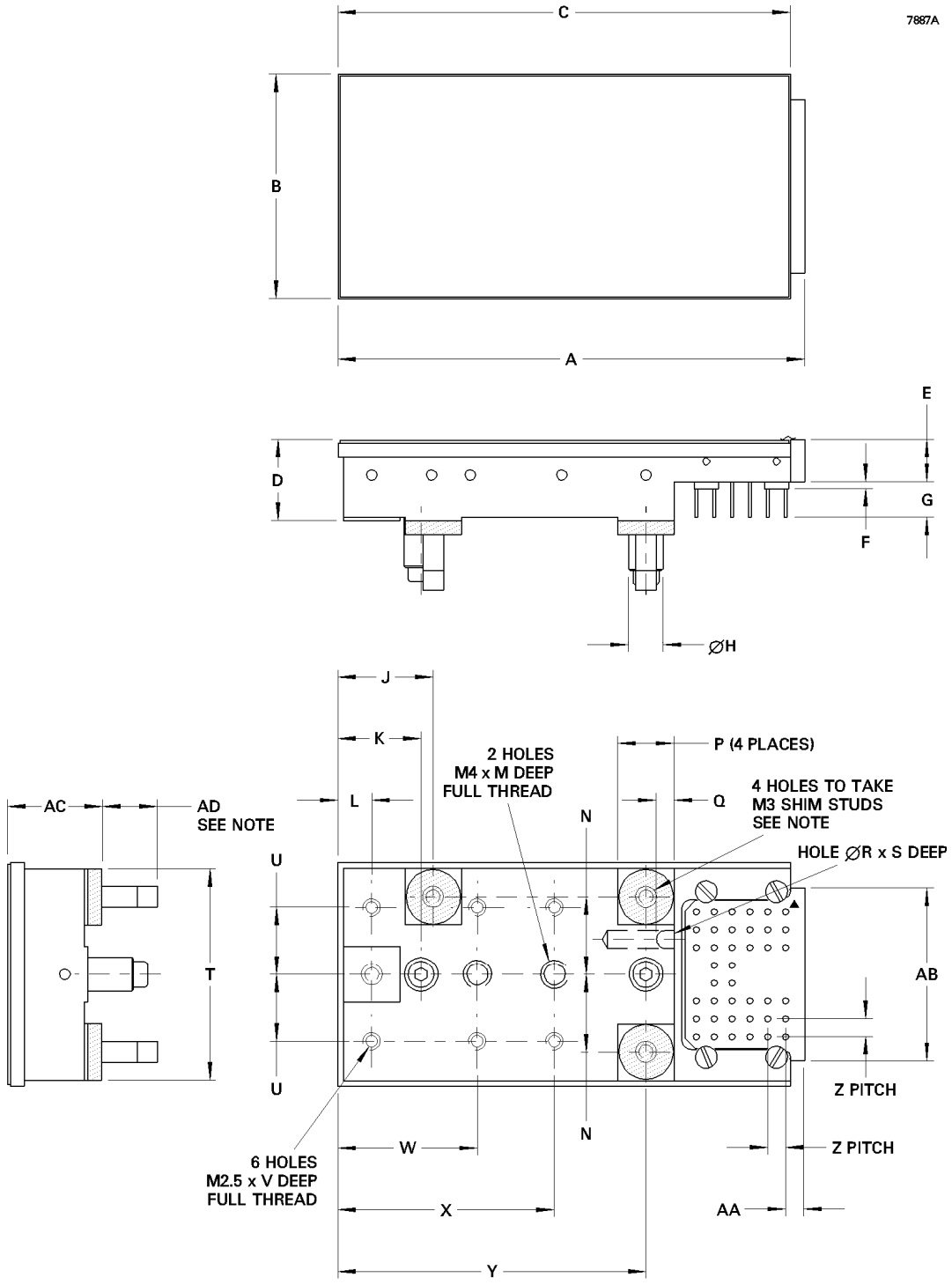
CLOCK TIMING REQUIREMENTS

Symbol	Description	Minimum	Typical	Maximum	Units
T_i	Image clock period	50	100	(see note 14)	µs
t_{wi}	Image clock pulse width	25	50	(see note 14)	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	1	10	$0.5t_{oi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	10	$0.5\ t_{oi}$	µs
t_{oi}	Image clock pulse overlap	5	10	$0.2T_i$	µs
t_{li}	Image clock pulse, two phase low	10	20	$0.2T_i$	µs
t_{dir}	Delay time, I∅ stop to R∅ start	10	20	(see note 14)	µs
t_{dri}	Delay time, R∅ stop to I∅ start	1	2	(see note 14)	µs
T_r	Output register clock cycle period	1	(see note 15)	(see note 14)	µs
t_{rr}	Clock pulse rise time (10 to 90%)	100	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	50	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	50	$0.1T_r$	$0.2T_r$	ns
t_{rx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.2T_r$	ns
t_{dx}	Delay time, ∅R low to R∅3 low	50	$0.5T_r$	$0.8T_r$	ns

NOTES

14. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
15. As set by the readout period.

PACKAGE DETAIL



Ref	Millimetres
A	66.64 max
B	31.72 ± 0.01
C	64.28 ± 0.01
D	11.65
E	6.00
F	1.00
G	5.00
H	4.800 ± 0.005
J	13.55
K	11.80
L	4.80
M	6.00 min
N	11.00
P	8.00
Q	2.50
R	2.50
S	6.50
T	30.00
U	9.50
V	5.50 min
W	19.80
X	30.80
Y	43.80
Z	2.54
AA	2.70
AB	24.5
AC	14.00 ± 0.01
AD	8.50 ± 0.01
	15.00 ± 0.01

Outline Note

The device is supplied with shim studs to hold it onto the customer's mounting plate, fitted to three of the four holes as required. The studs are available in two lengths (see dimension AD). The default unless specified is the 8.50 mm stud in the offset position.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving sockets to be positively grounded

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (i.e. all CCD pins except SS, DD, RD, OD and OS) but not to the other pins.

The devices are assembled in a clean room environment. e2v technologies recommend that similar precautions are taken to avoid contaminating the active surface.

HIGH ENERGY RADIATION

Performance parameters will begin to change if the device is subject to ionising radiation. Characterisation data is held at e2v technologies with whom it is recommended that contact be made if devices are to be operated in any high radiation environment.

TEMPERATURE RANGE

Operating temperature range ..... 153 - 323 K
Storage temperature range ..... 73 - 373 K

Full performance is only guaranteed at the nominal operating temperature of 173 K.

Operation or storage in humid conditions may give rise to ice on the surface when the sensor taken to low ambient temperatures, thereby causing irreversible damage.

Maximum rate of heating or cooling ..... 5 K/min